ABSTRACT OF THE DISCLOSURE

A memory cell architecture is provided herein for increasing memory speed, performance and robustness within a highly compact memory cell layout. Though only a few embodiments are provided herein, a feature common to all embodiments includes a novel means for sharing one or more contact structures between vertically adjacent memory cells. In particular, one or more contact structures may be shared unequally between two vertically adjacent memory cells for reducing a vertical dimension, or length, of the memory cell. Other features are disclosed for producing the highly compact memory cell layout. The various features of the present invention may be combined to produce high-performance, high-density memory arrays.